AND8241/D

A 5.0 V/2.0 A Standby Power Supply for INTEL Compliant ATX Applications

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ATX power supply units (PSU) require a standby section who keeps alive some particular areas of the motherboard. Among the live sections are the USB ports, the Ethernet controller and so on. The INTEL ATX Power Supply Design Guide 2.01 (rev. June 04) describes the standby voltage rail needed for this purpose. This is the +5.0 VSB section (3.3.3):

- Output voltage: 5.0 V, ±5%
- Nominal load current: 2.0 A
- 500 ms pulses current (USB wake-up event): 2.5 A
- Input power less than 1.0 W at 230 Vac for an output power of 500 mW
- Power on time: 2.0 s maximum
- Short circuit protection with auto-recovery

On top of these requirements, most of PSU designers use the standby power supply as an auxiliary rail to power the main controller. This is an auxiliary 12-13 V rail or, if an UC384X is implemented, this rail can go up to 20 V. When put in standby, a small switch shuts down the controller by interrupting this rail.

To help designers quickly fulfilling the above needs, the NCP1027 has been introduced. This DIP 8 package hosts a high performance controller together with a low $R_{DS(on)}$ 700 V BVdss MOSFET. On top of the standby needs, we have packed other interesting goodies in this circuit. They are summarized below:

- *Brown-out detection:* the controller will not allow operation in low mains conditions. You can adjust the level at which the circuit starts or stops operation.
- *Ramp compensation:* designing in Continuous Conduction Mode helps to reduce conduction losses. However, at low input voltage (85 Vac), the duty-cycle might exceed 50%, and the risk exists to enter a

subharmonic mode. A simple resistor to ground injects the right compensation level.

- *Over Power Protection:* a resistive network to the bulk reduces the peak current capability and accordingly harnesses the maximum power at high line. As this is done independently from the auxiliary V_{CC}, the design gains in simplicity and execution speed.
- *Latch-off input:* some PC manufacturers require a complete latch-off in presence of an external event, e.g. overtemperature. The controller offers this possibility via a dedicated input.
- *Frequency dithering:* the switching frequency (here 65 kHz) is modulated during operation. This naturally spreads the harmonic content and reduces the peak value when analyzing the signature.

Design Description

A full CCM operation gave us an adequate performance in this particular case, with good full load efficiency results as we will see. The part switches at 65 kHz which represents a good trade-off between switching losses and EMI control. A brown-out circuit was implemented, turning the SMPS on around 80 Vac and turning it off at 60 Vac. Different values can easily be selected by altering the dedicated resistive network. Please note that this network impedance has a direct influence on the standby power. To limit the amount of current the supply can deliver at high line, it is necessary to limit the propagation delay effects. The NCP1027 hosts an exclusive circuitry used to reduce the maximum peak current as the line increases. We will see that, once implemented around the auxiliary diode, it does not affect the standby power and nicely harnesses the maximum power. The electrical schematic of the board appears on Figure 1.
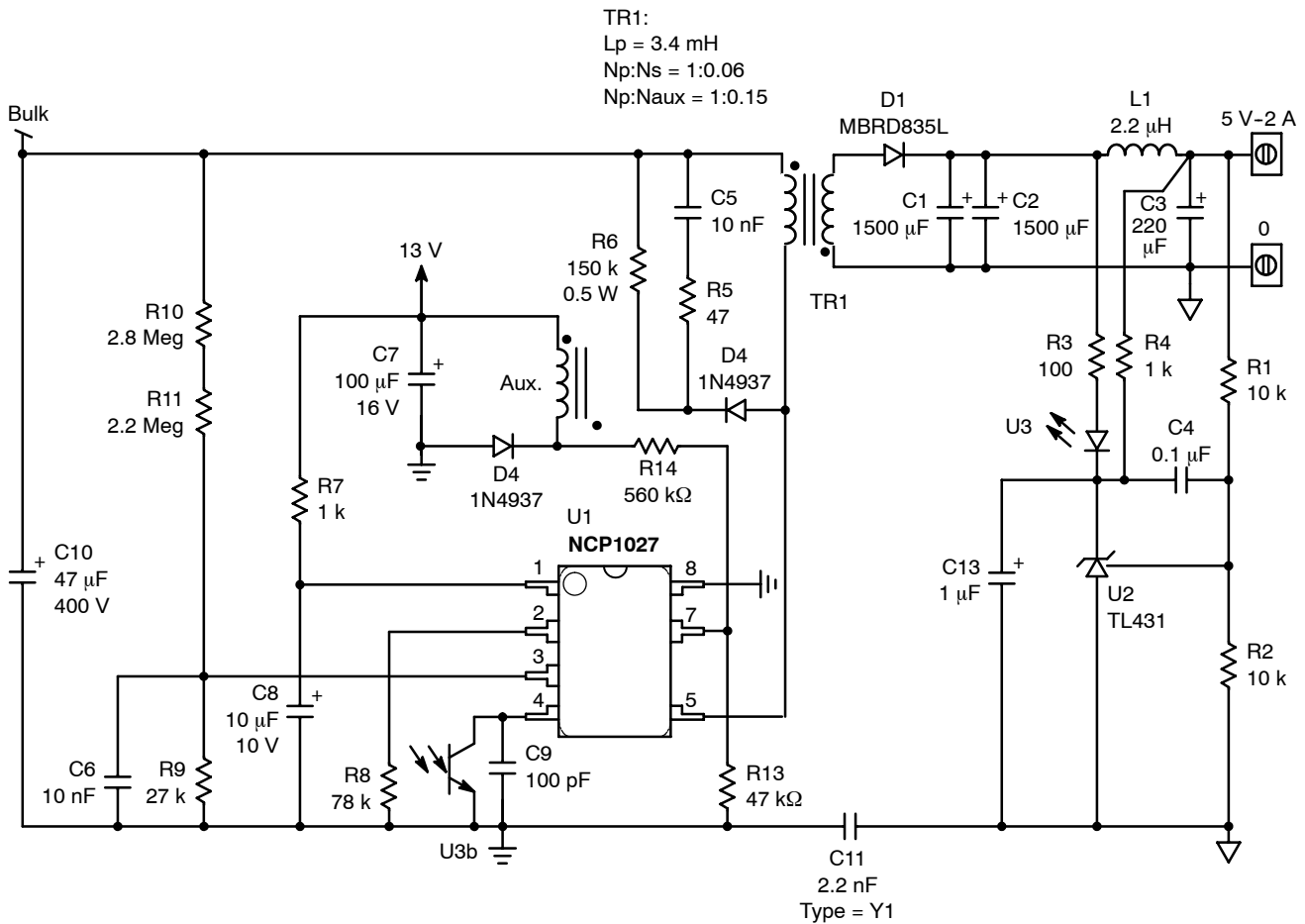
Figure 1. The application board electrical schematic without the EMI filter for simpler representation.

Let us start the review by the transformer description.

Transformer

The design of the transformer section represents the most difficult part as standby power in no-load and 0.5 W output must be respected. Various iterations have lead us to adopt the following characteristics:

Lp = 3.4 mH

Np:Ns_power = 1:0.06

Np:Ns_aux = 1:0.152

The auxiliary winding in this case delivers 12.5 V but it can be set to any other value, depending on the main controller V_{CC}. The turn ratio limits the reflected value on the drain to less than 100 V, without risks of biasing the MOSFET body diode at the lowest input voltage. This transformer is available from Coilcraft under a reference detailed in the Bill Of Material (BOM).

As we have seen, our design operates in CCM at full load but obviously enters the Discontinuous Conduction Mode (DCM) at light loads. The transition point can be evaluated using the following formula:

$$R_c = 2L_p N^2 F_{sw}\left(\frac{NV_{in} + V_{out}}{NV_{in}}\right)^2 \qquad \text{(eq. 1)}$$

where:

L_p, the primary inductance, 3.4 mH

N, the turn ratio, 0.06

F_{sw}, the switching frequency, 65 kHz

V_{in}, the input voltage

V_{out}, the output voltage

Calculations lead to the following mode transition load values:

Lowest line, V_{in} = 120 Vdc: R_c = 4.56 Ω or Iout = 1.0 A

Highest line, V_{in} = 370 Vdc: R_c = 2.4 Ω or Iout = 2.0 A

Please note that low line is actually 85 Vac but the ATX PSU including a large bulk capacitor, we can neglect the ripple given the low output power of this converter, hence a 120 V value. At the highest line, the design operates at the boundary between CCM and DCM. The duty-cycle at full load and lowest input line can be evaluated via the flyback static transfer function:

$$D = \frac{V_{out}}{NV_{in} + V_{out}} \qquad \text{(eq. 2)}$$

The highest duty-cycle is found to be 41%. However, this number is likely to increase a little, given the presence of the leakage inductance.

Ramp Compensation

Being in CCM with a duty-cycle close to 50% (or above 50% in transient conditions), we need ramp compensation. Several ways exist to evaluate the amount of ramp compensation. The quickest one evaluates the *off* slope of the secondary inductance and injects around 50% of this slope through a compensating ramp (S_a) into the controller. With the NCP1027, the ramp compensation level is set via a simple resistor connected from pin 2 to the ground, as shown in Figure 1.

We can calculate the *off* slope, the one actually needed to evaluate S_a, by reflecting the output voltage over the primary inductance. The slope is projected over a complete switching period.

$$S_{off} = \frac{V_{out} + V_f}{NL_p} T_{sw} = \frac{6 \times 15\,\mu}{0.06 \times 3.4\,m} = 441\,mA/15\,\mu s \quad \text{(eq. 3)}$$

The NCP1027 features a current-mode architecture using a SENSEFET™ device. That is to say, the controller does not directly sense the current via a resistor but through a Kelvin cell. For this particular circuit, the cell ratio can be modeled as an equivalent sense resistor of 350 mΩ. This current slope will thus become a voltage slope having a value of:

$$S'_{off} = 0.441 \times 0.375 = 165\,mV/15\,\mu s \quad \text{(eq. 4)}$$

If we chose 50% of this down slope, then the final compensation ramp will present a slope of:

$$S_a = \frac{S'_{off}}{2} = 83\,mV/15\,\mu s = 5.53\,kV/s \quad \text{(eq. 5)}$$

Following the data sheet indications, we evaluate the resistor value to be:

$$R_{ramp} = \frac{7562}{0.083} = 91\,k \quad \text{(eq. 6)}$$

In case no ramp compensation is required, pin 2 must be tied to V_{CC}, the adjacent pin. As experiments were carried at lower input voltages (C_{bulk} is small on the demo board), it was decided to slightly increase the amount of ramp compensation by reducing R_{ramp} to 78 kΩ.

Over Power Protection (OPP)

Power supply controllers sensing the primary current to check whether it goes over a certain limit often face propagation delay problems. That is to say, despite the current limit detection by a dedicated comparator, the information takes a certain amount of time to propagate through the logic circuits and eventually reset the latch. During this time, the primary current keeps increasing by a rate given by the primary inductance and the input voltage. Hence, we can quickly see the effects of a 100 ns delay at high line or low line:

$$I_{final} = I_{peak\_max} + \frac{V_{in}}{L_p} t_{prop} \quad \text{(eq. 7)}$$

If the limit is set to 750 mA, then we have:

$$I_{final} = 750\,m + \frac{100}{3.4\,m} 100\,n = 753\,mA \quad \text{(eq. 8)}$$

$$I_{final} = 750\,m + \frac{374}{3.4\,m} 100\,n = 761\,mA \quad \text{(eq. 9)}$$

The difference looks small but it often leads to a significant different in output current capabilities, especially with larger propagation delays. Hence, the need to act in high line conditions via a dedicated circuitry.

The NCP1027 hosts a special section used to reduce the maximum peak current limit as the mains increases. The system works by connecting a resistive network to the bulk capacitor, as Figure 2 depicts:
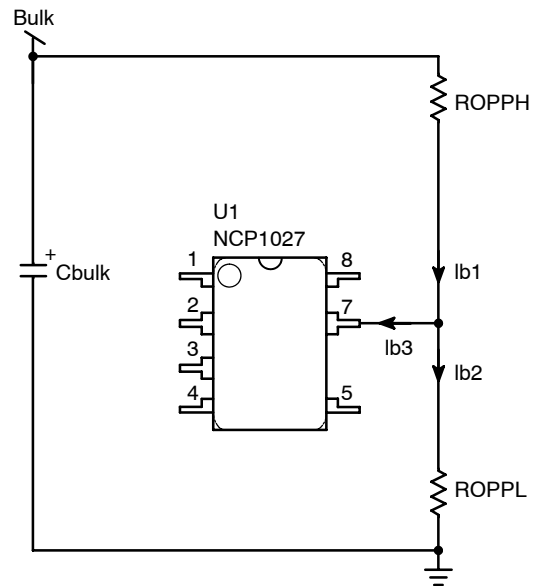

Figure 2. A possible option to reduce the peak excursion consists of connecting a resistive divider to the bulk capacitor.

By injecting a current I_{b3} proportional to V_{bulk}, the maximum peak current limits reduces. Analytically obtaining the right value for I_{b3} might represent a complicated exercise as many parameters play a role. To the opposite, a simple experimental method can be setup to obtain the value of the needed current:

1. Configure your working power supply as suggested by Figure 3 or 4. These figures are purposely simplified for ease of understanding of the added circuitry. Figure 3 represents the safest way to run the measurement as the dc power supply injects current via an optoisolator without sharing the converter's ground. An amp-meter is inserted to read the current I_{b3}. Leave the dc bias to zero for now.
2. Power the converter and set the input voltage to the highest of your specification. Let us assume it is 375 Vdc.

3. Increase the output current to the point where the system should shut down per specification. Let's say 3.2 A for this design.
4. Start to increase the variable power supply dc voltage until the amp-meter deviates. Increase carefully because you deal with hundred of μA only.

5. At a certain time, if you continue to increase the current in pin 7, the converter enters in protection mode. The current flowing in pin 7 and the voltage on it prior to the shutdown, correspond to the variables you look for. In this example, we measured a V_f voltage of 2.45 V and a current of 31 μA.
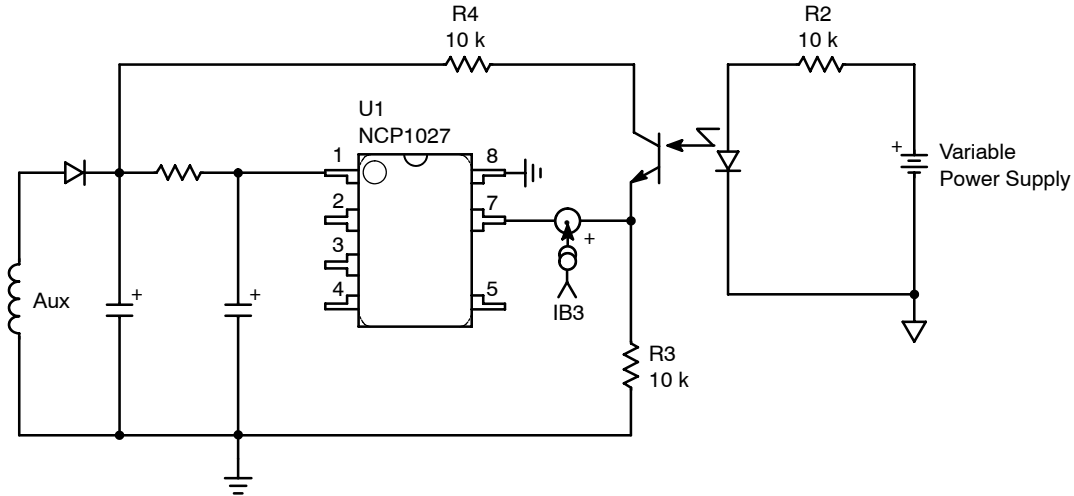
Figure 3. An isolated way to safely inject current into pin 7 at high line.
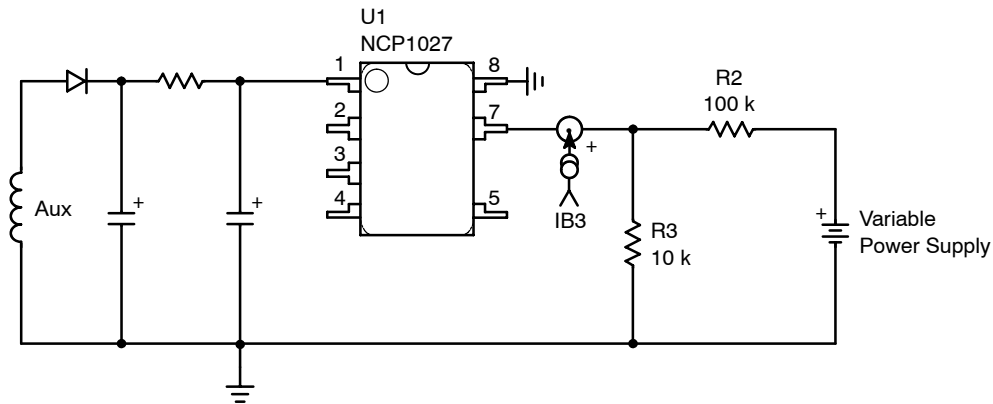
Figure 4. A non-isolated way to inject current into pin 7 at high line.

The preliminary curve showing the relationship between the injected current and the maximum peak current setpoint appears in Figure 5. We can see that 31 μA corresponds to a 20% reduction in the maximum peak current capability. The V_f parameter specifies the voltage at which pin 7 starts to pump in current. It is around 2.5 V as we can see it.
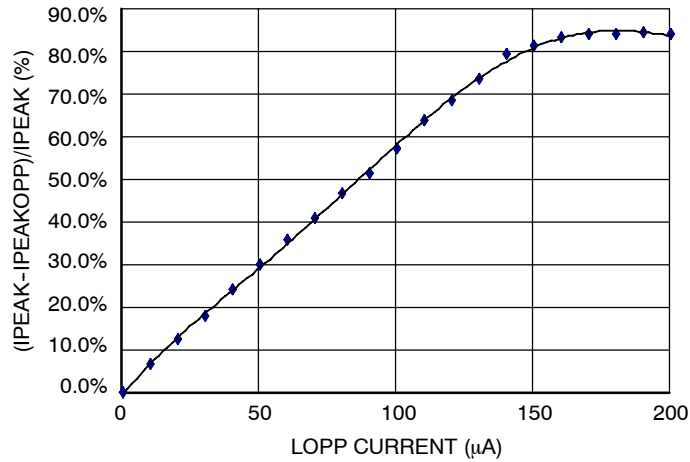
**Figure 5. Maximum Peak Current Setpoint Reduction
vs. Pin 7 Injected Current**

To compute the resistor values, we need to define the range within which the OPP reduction should activate. As we do not want any OPP action at low input voltages, we will select resistors to start reducing at V_{in} = 200 Vdc, with a clamp at V_{in} = 375 Vdc. Using the following equations and our collected data leads us to the final values:

V_{bulkH} = 375 Vdc
V_{bulkL} = 200 Vdc
I_{OPP} = 31 μA
V_f = 2.45 V

$$R_{OPPL} = \frac{V_{bulkH}-V_{bulkL}}{I_{OPP}(V_{bulkL}-V_f)}V_f = 70 \text{ k}\Omega \quad \text{(eq. 10)}$$

$$R_{OPPH} = R_{OPPL}\frac{V_{bulkL}-V_f}{V_f} = 5.6 \text{ M}\Omega \quad \text{(eq. 11)}$$

Unfortunately, despite the good behavior of the network, its permanent presence on the bulk rail will affect the consumption in standby. When you chase every hidden milli-watt, it can become a nasty problem. To avoid this trouble, a simple solution around the auxiliary winding can be worked out. This is presented in Figure 6. During the on time, where the power switch is turned on, the input voltage appears across the primary transformer. Given the auxiliary diode configuration, $N \cdot V_{in} + V_{out}$ also appears on the cathode, N being the primary to secondary turn ratio. As this voltage moves up and down with the bulk level, we can perfectly use it for our OPP purposes. Due to its pulsating low voltage nature, power consumption will be the smallest.
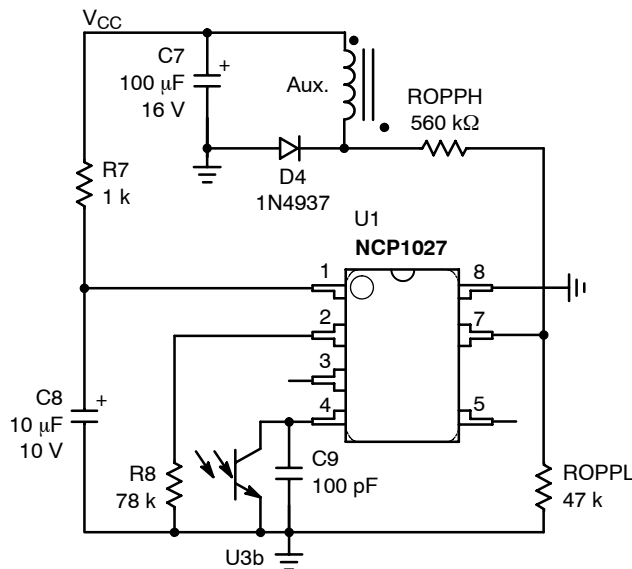
**Figure 6. The auxiliary diode lends itself very well to
a cheap and energy efficient OPP implementation.**

Hooking an oscilloscope probe on D_4 cathode gives us the bulk image evolution between its minimum and maximum values. We can then run the calculation again to obtain R_{OPPH} and R_{OPPL}:

V_{bulkH} = 55 Vdc
V_{bulkL} = 37 Vdc
I_{OPP} = 31 μA
V_f = 2.45 V

R_{OPPH} = 580 kΩ → 560 kΩ after tweak
R_{OPPL} = 41 kΩ → 47 kΩ after tweak

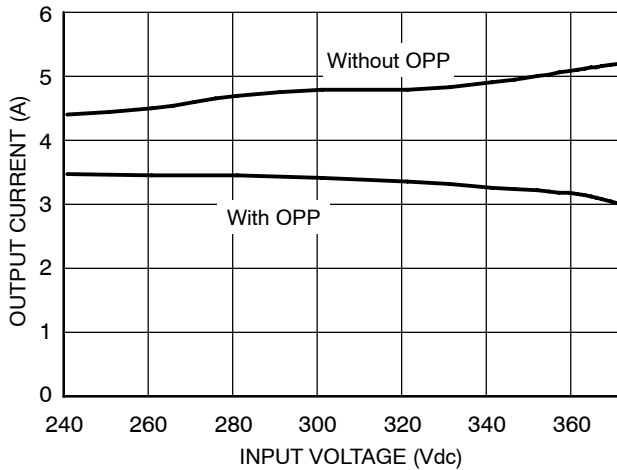Figure 7 shows the results before and after OPP implementation. The output current stays below 3.5 A in all cases which is well within specs.

Figure 7. Over Power Protection at work keeps the output current below 3.5 A.

Brown-out

Brown-out (BO) detection offers a means to protect the converter in presence of low input voltages by stopping switching operation until the mains comes back to a normal value. The circuit works by observing a fraction of the bulk level via a resistive divider routed to pin 2. When the level on pin 2 lies below 0.6 V, the controller does not allow switching operation, but the high-voltage current source maintains the V_{CC} on pin 1. Then, as soon as pin 2 voltage crosses 0.6 V, the V_{CC} is ready to power the chip and switching can start. As this occurs, pin 2 injects around 12 μA (I_{BO}) in the resistive bridge to create a hysteresis. The designer must thus select the turn-on and turn-off voltages to further apply the following equations:

$$R_{upper} = R_{lower} \frac{V_{bulk1} - V_{BO}}{V_{BO}} \qquad \text{(eq. 12)}$$

$$R_{lower} = V_{BO} \frac{V_{bulk1} - V_{bulk2}}{I_{BO} \times (V_{bulk1} - V_{BO})} \qquad \text{(eq. 13)}$$

Suppose we want to start at V_{in} = 110 Vdc (77 Vac) and stop operation at V_{in} = 70 Vdc (50 Vac), then applying Equations 12 and 13 leads to the following values:

R_{upper} = 4.0 MΩ
R_{lower} = 22 kΩ

Total power dissipation at nominal line is then

$$P_{BO} = \frac{330^2}{4.02 \text{ Meg}} = 27 \text{ mW.}$$

On the board, we purposely modified these values to further improve the standby power.

Auxiliary Winding

The auxiliary winding is set to deliver 13 V nominal when the converter is fully loaded. To avoid any V_{CC} drops during transient loading, e.g. sudden load removal, the main V_{CC} capacitor C_7 has been increased to 100 μF, leading to a stable V_{CC} in no-load conditions. The resistor R_7 sets the Overvoltage Protection (OVP) level by adjusting the injected current in pin 1 internal shunt in case of problems. With 1.0 kΩ, the OVP level is set to V_{OVP} = 1.0 k · 7.0 m + 8.7 = 15.7 V typical on the auxiliary winding. Different values can be obtained by changing the resistor values or the ratio between the power and auxiliary windings.

Clamping Section

The converter uses an RCD clamp to safely limit the voltage excursion on the MOSFET drain. Failure to keep $V_{ds}(t)$ below 700 V will permanently damage the circuit. In application where the input line can be subject to strong high-voltage parasitic pulses, we recommend the usage of a Transient Voltage Suppressor (TVS), that will hard clamp all potentially lethal spikes on the drain. Figure 8 portrays the way to wire the TVS. Finally, the TVS offers superior performance in standby power compared to the RCD clamp. Simply because the RCD clamp always activates since the capacitor discharges via the resistor R as soon the leakage inductance is reset. Unfortunately, even in standby, this mechanism generates light losses. If you want to further save 50 mW, a TVS is of good usage. A 200 V TVS has shown to be a good solution here. You can use the 1.5KE200A from ON Semiconductor for instance.
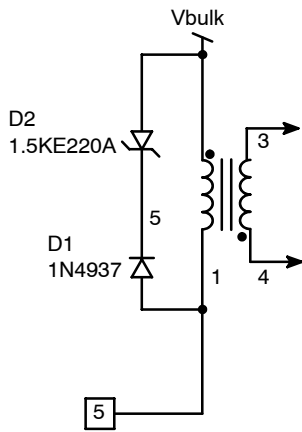
Figure 8. A TVS must be used if the input voltage can be subject to high voltage spikes.
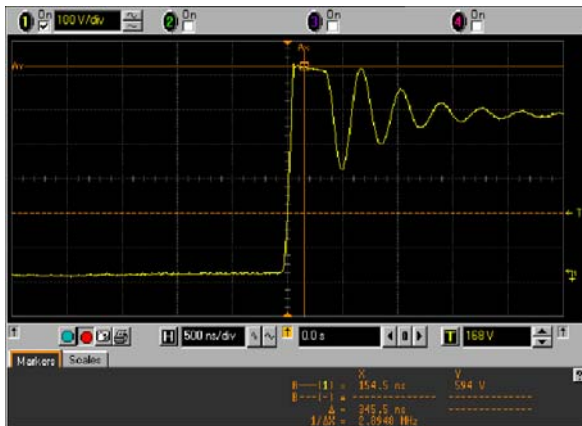

Figure 9. Always check the voltage on the drain at the highest line condition (265 Vac).

Secondary Side

The secondary side uses a Schottky diode featuring an 8.0 A capability and a breakdown voltage of 35 V. This is enough since high line conditions imply a Peak Inverse Voltage (PIV) of:

$$PIV = NV_{in} + V_{out} = 0.06 \times 370 + 5 = 27.2 \text{ V}$$

(eq. 14)

The forward voltage V_f goes down to 0.41 V @ $T_j = 125°$ which, neglecting ohmic losses, induces conduction losses of:

$$P_{diode} = I_{RMS}{}^2 R_d + I_{avg}V_f \approx 2 \times 0.41 = 0.8 \text{ W}$$

(eq. 15)

The output capacitor C_{out} is selected to a) pass the adequate RMS current b) limit the undershoot ΔV when the output is banged by a current step ΔI. The undershoot depth of a closed-loop converter having a bandwidth f_c can be evaluated via the following formula:

$$\Delta V = \frac{\Delta I}{f_c C_{out}}$$

(eq. 16)

Calculations gave us a value of 2.4 mF, made of two low-impedance 10 V/1200 μF capacitors.

A TL431 ensures a stable regulation at 5.0 V via a type-2 amplifier. R_3 and the NCP1027 internal pullup resistor set the midband gain, whereas C_4 sets the zero position. The small capacitor C_9 filters out residual noise and adds a high frequency pole, acting together with the optocoupler one. The step load response is clean, without any ringing at both high and low line conditions. The circuit can be slightly modified to add some more soft-start, in case designers would fear output overshoots. Figure 10 shows how to connect a 1.0 μF/10 V capacitor to soften the start-up sequence:
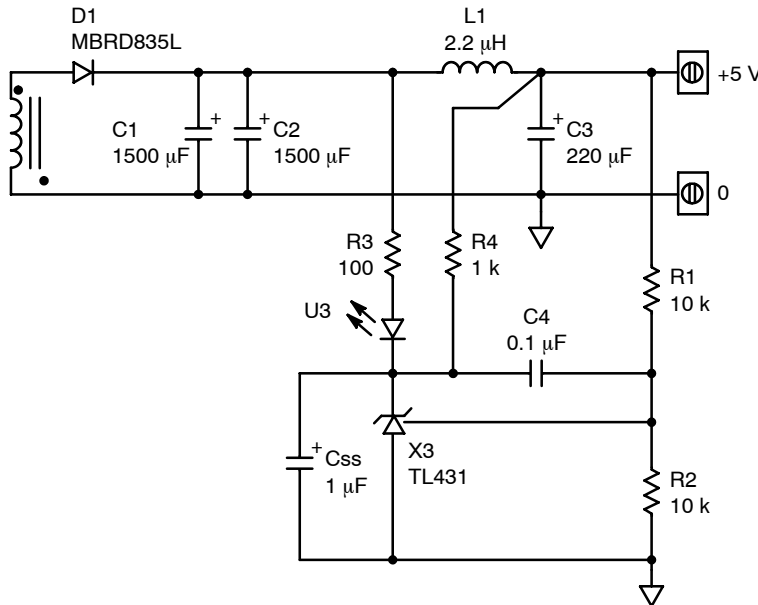
Figure 10. A 1.0 μF capacitor connected on the TL431 strengthens the startup sequence.

The basic description being done, let us have a look at the board performance. Standby measurements were captured with a Yokogawa WT210 on a board after it warmed up for 15 minutes. Please make sure the WT210 volt-mater is placed before the current shunt, otherwise its input impedance will degrade the low-power measurements by 30 mW at high line.

Static Measurements
V_{in} = 230 Vac
$T_{ambient}$ = 25°C

P_{out} = 0 P_{in} = 88 mW V_{aux} = 10.14 V
P_{out} = 0.5 W P_{in} = 779 mW V_{aux} = 11.64 V η = 64.2%
P_{out} = 10 W P_{in} = 12.3 W V_{aux} = 12.14 V η = 81.3%

→ Please note that replacing R_6 by a 200 V TVS as mentioned in the text, reduces the input power at 0.5 W @ 230 Vac down to 715 mW and 73 mW at no load.

P_{out} = 0 P_{in} = 98 mW at V_{in} = 265 Vac with RCD
P_{out} = 0 P_{in} = 85 mW at V_{in} = 265 Vac with TVS

T_{case} NCP1027 = 50°C at P_{out} = 10 W

Short-circuit temperature: NCP1027 T_{case} = 42°C, T_{diode} = 52°C
Maximum output current: 3.0 A @ 265 Vac

V_{in} = 85 Vac
$T_{ambient}$ = 25°C

P_{out} = 0 P_{in} = 54 mW V_{aux} = 10.15 V
P_{out} = 0.5 W P_{in} = 704 mW V_{aux} = 11.6 V η = 71%
P_{out} = 10 W P_{in} = 12.6 W V_{aux} = 12.6 V η = 79.5%

T_{case} NCP1027 = 60°C at P_{out} = 10 W

Short-circuit temperature: T_{case} NCP1027 = 44°C, T_{diode} = 52°C
Maximum output current: 3.1 A

Dynamic Measurements
Some critical waveforms have been captured on the demonstration board and are reproduced below:
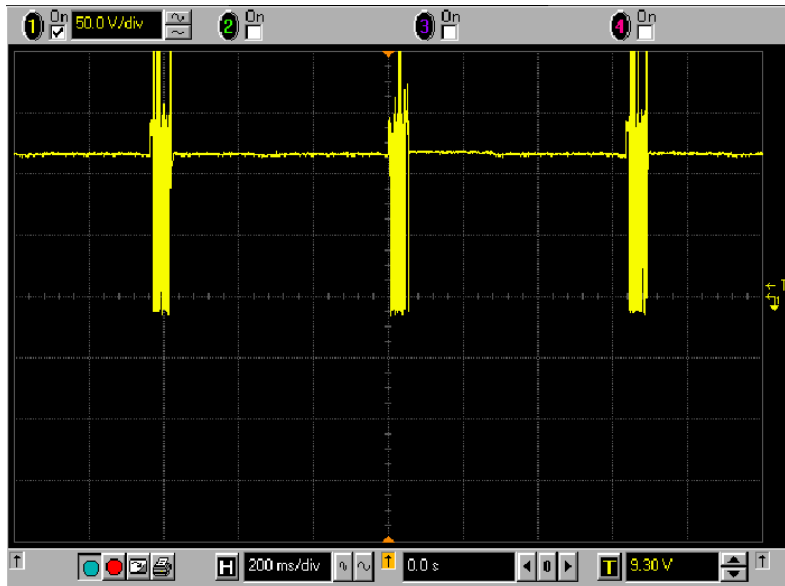
Figure 11. Short-Circuit Protection, Drain-Source Waveform

In Figure 11, we can see the power supply operating in a so-called hiccup mode, trying to re-start as soon as the internal timer has elapsed. The resulting duty-burst stays below 8%, keeping all component temperatures at a moderate level. This is an auto-recovery type of protection, implying a re-start when the fault is removed (V_{in} = 230 Vac).
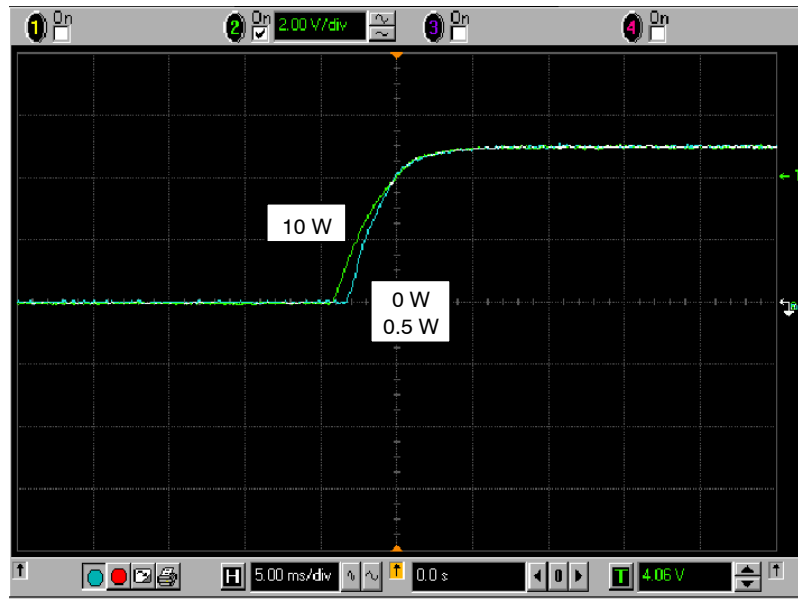
Figure 12. Startup Sequence at Three Loading Conditions

Figure 12 shows a typical startup sequence, captured at different output levels (0, 0.5 W and 10 W) for $V_{in} = 85$ Vac. Changing the input voltage does not modify the shape of the waveform. This waveform has been captured with the 1.0 μF wired as suggested by Figure 10.
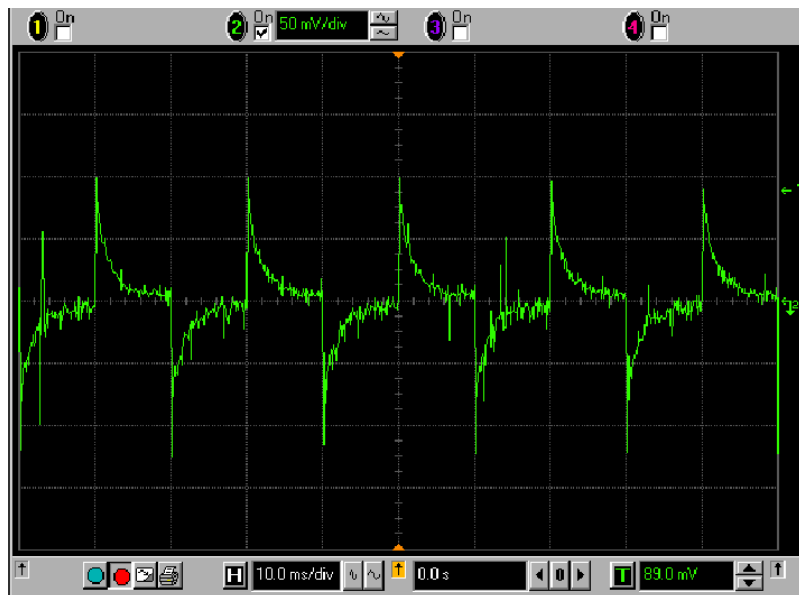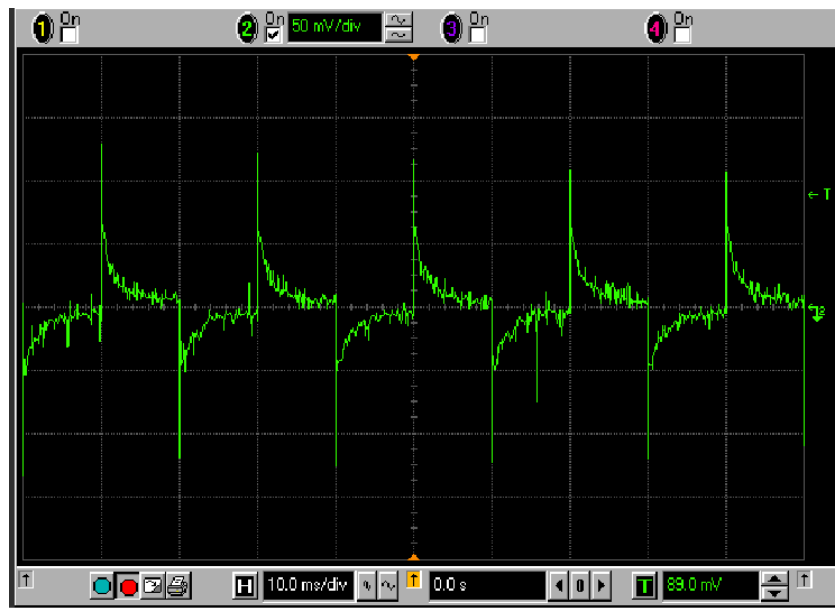

Figure 13. Load step where V_{out} is banged from 0.1 A to 2.5 A with a 1.0 A/μs slew-rate (V_{in} = 85 Vac).

**Figure 14. Load step where V$_{out}$ is banged from 0.1 A to 2.5 A with a
1.0 A/µs slew-rate (V$_{in}$ = 230 Vac).**

Figures 13 and 14 represent the step load response from the standby mode to the wake-up mode, featuring a variation from 100 mA up to 2.5 A. The spike you can see on the waveforms comes from the current discontinuity indured by the LC filter inductor L_1.
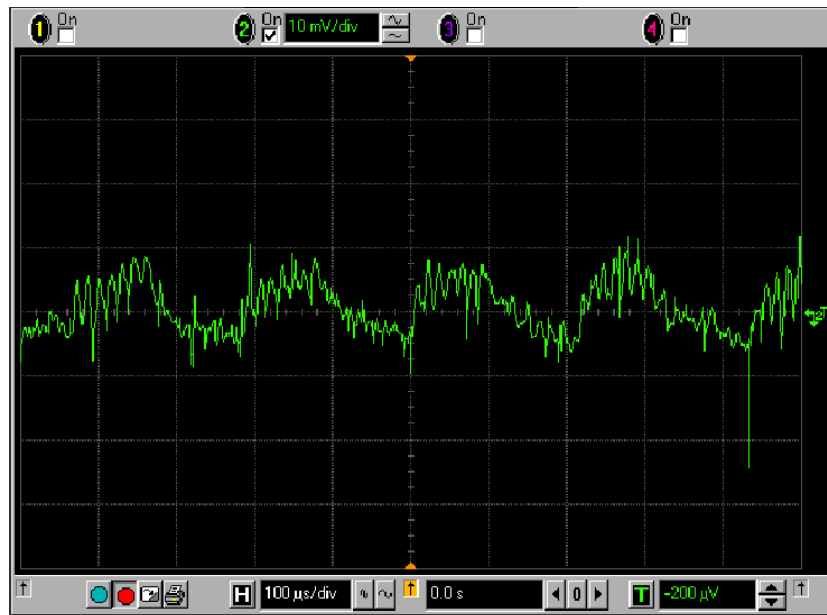
Figure 15. Peak-to-peak ripple, P$_{out}$ = 0.5 W, Cable length = 30 cm, V$_{in}$ = 85 Vac.

Figure 16. Peak-to-peak ripple, P_{out} = 0.5 W, Cable length = 30 cm, V_{in} = 230 Vac.

Figures 15 and 16 display the ripple amplitude when the board enters skip cycle, mainly at a 0.5 W output power. The measurement has been carried at two line levels and using 30 cm long cables to mimic a real PSU cabling connector.
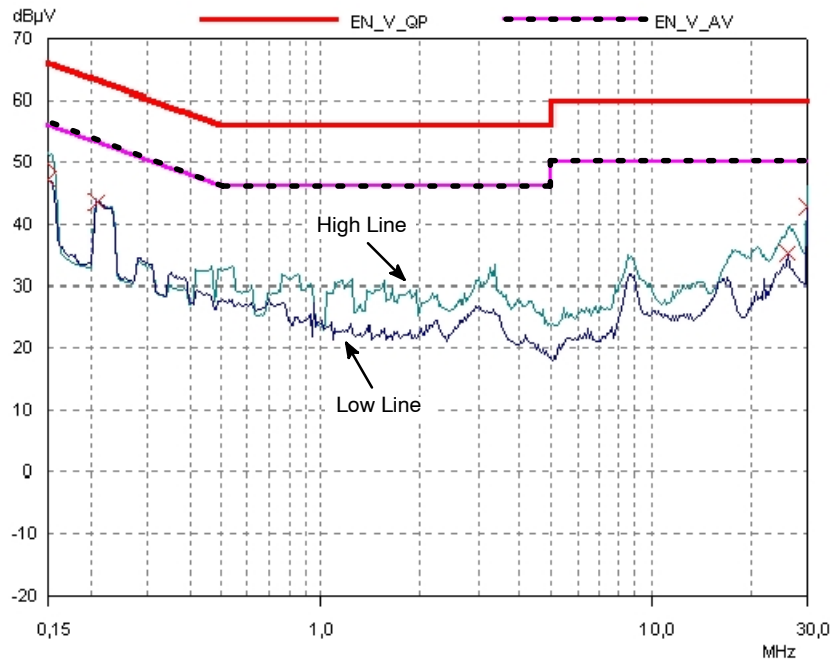
Figure 17. EMI signature, low line and high line in quasi-peak, P_{out} = 10 W.

Figure 17 shows the advantage of EMI jittering, offering a clean signature at both line levels. As the sweep is successfully made in Quasi-Peak (QP) it implies immediate compliance in average mode.
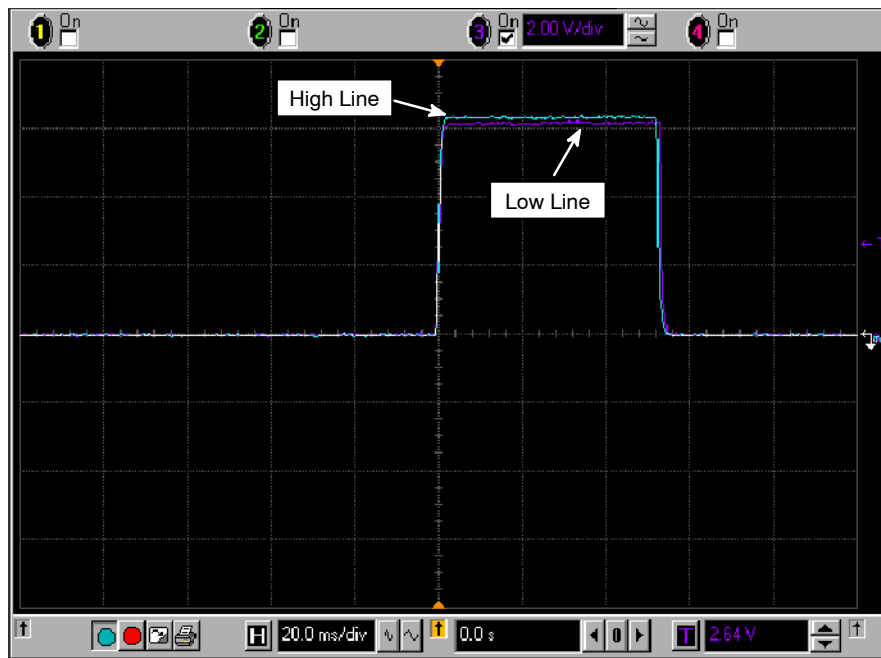
Figure 18. Peak Output Current in Short−Circuit at Both Line Conditions: 6.3 A
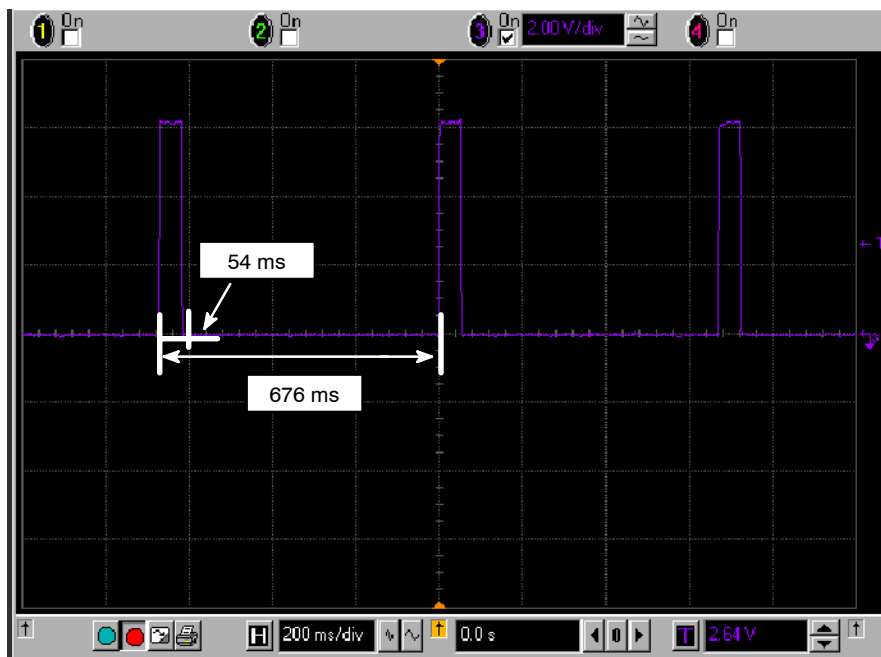
Figure 19. Output Current Waveform in Short−Circuit

Some PC application specs require the output average and RMS currents in short−circuit to stay within given limits. With this design, we have obtained the following results at high−line:

- I_{peak} = 6.4 A
- $I_{out,av}$ = 6.4 x 54 / 676 = 511 mA

- $I_{out,rms}$ = $6.4 \sqrt{\dfrac{54}{676}}$ = 1.8 A

PCB Views

The PCB routing includes large copper areas around the integrated circuit to maximize its power dissipation. The diode is placed on the copper side and due to its low V_f, it leads to good thermal performance.
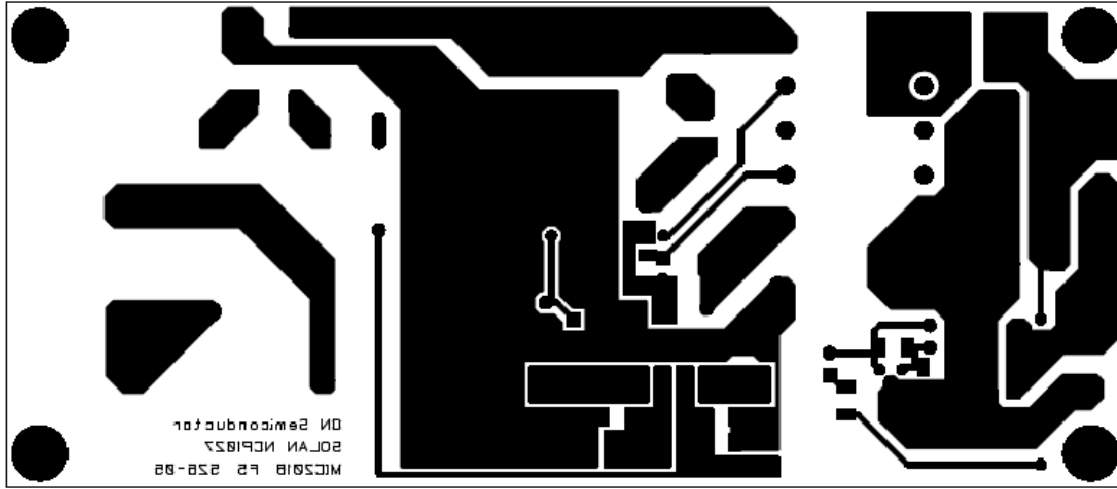
Figure 20. The PCB Copper Area of the Demonstration Board
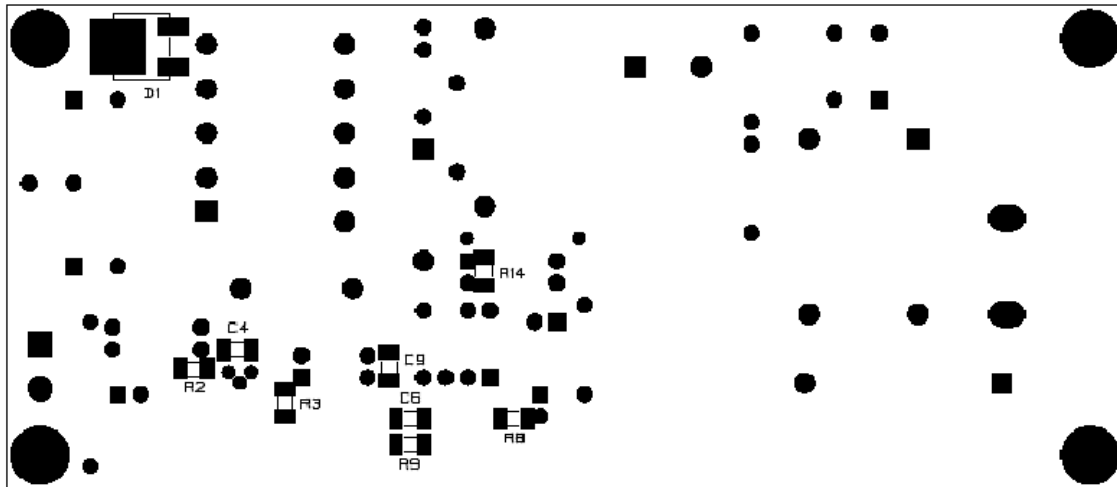
Figure 21. The SMD Positions on the Copper Side
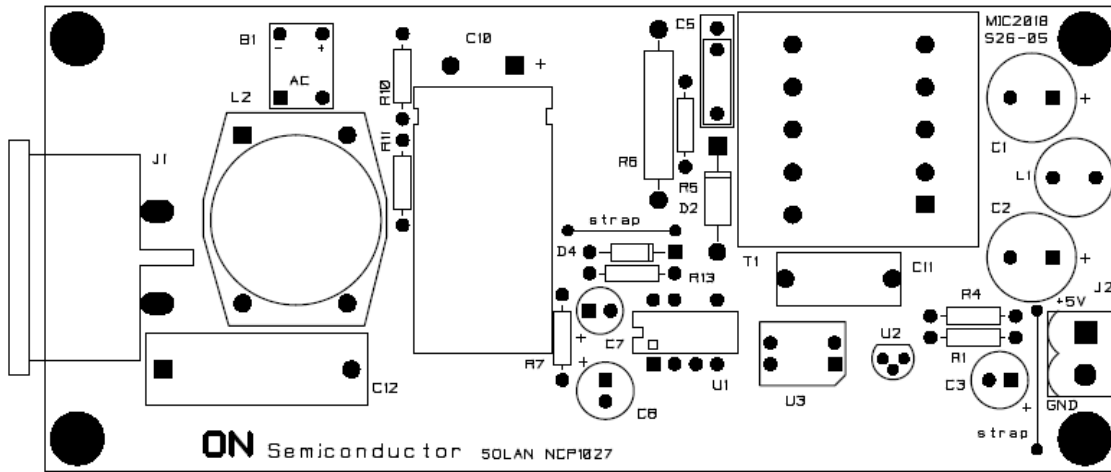
Figure 22. Component Side View

Bill of Material

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
B1	1	Single–Phase Bridge Rectifier	800 V	NA		General Semiconductor	DF08M	Yes	No
C1,C2	2	Radial Lead Electrolityc Capacitor	1200 µF/16 V	20%		Panasonic	EEUFC1C122	Yes	
C10	1	Radial Lead Electrolityc Capacitor	47 µF/400 V	20%		Panasonic	ECA2GHG470	Yes	
C11	1	Capacitor, Y1 Class	2.2 nF/400 V	20%		Vishay	WKP222	No	
C12	1	Capacitor, X2 Class	220 nF/275 V	20%		Evox Rifa	PHE840MX6220M	No	
C13	1	Radial Lead Electrolityc Capacitor	1 µF/50 V	20%		Panasonic	EEUFC1H1R0	Yes	
C3	1	Radial Lead Electrolityc Capacitor	220 µF/16 V	20%		Panasonic	EEUFC1C221	Yes	
C4	1	SMD Capacitor	100 nF	10%	1206	Epcos	B37872–K5104–K60	Yes	
C5	1	Polyester Chip Capacitor	10 nF/630 V	10%		Vishay	MKT1822–310	Yes	
C6	1	SMD Capacitor	10 nF	10%	1206	Epcos	B37872–K5103–K60	Yes	
C7	1	Radial Lead Electrolityc Capacitor	10 µF/63 V	20%		Elna	RE3–63V100M	Yes	
C8	1	Radial Lead Electrolityc Capacitor	100 µF/10 V	20%		Panasonic	EEUFC1A101	Yes	
C9	1	SMD Capacitor	1 nF	10%	1206	Epcos	B37872–K5102–K60	Yes	
D1	1	Schottky Barrier Rectifier	35 V/8 A	NA	DPAK	ON Semiconductor	MBRD835L	Yes	Yes
D2,D4	2	Fast–Recovery Rectifier	600 V/1 A	NA		ON Semiconductor	1N4937	Yes	Yes
J1	1	PCB Connector	NA	NA		Multicomp	JR–201S	Yes	
J2	1	PCB Connector	NA	NA		Weidmuller	PM5.08	Yes	
L1	1	Inductor, 2.2 µH, 2.5 A	2.2 µH	NA		Wurth Elektonic	744772022	Yes	
L2	1	Common Mode Inductor, 2*27 mH	27 mH	NA		Schaffner	RN114–0,8/02	Yes	
R1	1	Axial Lead Resistor 1/4w	10 kΩ	5%		Neohm	CFR25J10K0	Yes	
R10	1	Axial Lead Resistor 1/4w	2.8 MΩ	5%		Neohm	CFR25J2M8	Yes	
R11	1	Axial Lead Resistor 1/4w	2.2 MΩ	5%		Neohm	CFR25J2M2	Yes	
R13	1	Axial Lead Resistor 1/4w	47 kΩ	5%		Neohm	CFR25J47K0	Yes	
R14	1	Axial Lead Resistor 1/4w	560 kΩ	5%		Neohm	CFR25J560K	Yes	
R2	1	SMD Resistor	10 kΩ	1%	1206	Vishay	CRCW1206101J	Yes	
R3	1	SMD Resistor	100 Ω	1%	1206	Vishay	CRCW1206100RJ	Yes	
R4	1	Axial Lead Resistor 1/4w	680 Ω	5%		Neohm	CFR25J680	Yes	
R5	1	Axial Lead Resistor 1/4w	47	5%		Neohm	CFR25J47	Yes	
R6	1	Axial Lead Resistor 1w	150 kΩ/1 W	5%		Neohm	CFR100J150K0	Yes	
R7	1	Axial Lead Resistor 1/4w	1 kΩ	5%		Neohm	CFR25J1K0	Yes	
R8	1	SMD Resistor	78 kΩ	1%	1206	Vishay	CRCW1206781J	Yes	
R9	1	SMD Resistor	27 kΩ	1%	1206	Vishay	CRCW1206271J	Yes	
U1	1	NCP1027	NA	NA	DIP8	ON Semiconductor	NCP1027	No	Yes
U2	1	Adjustable Shunt Regulator	2.5–36 V/ 1–100 mA	2.20%	TO92	ON Semiconductor	TL431	No	Yes
U3	1	Optocoupler	NA	NA	DIP4	Vishay	SFH615A	No	
T1	1	Transformer	NA	NA		Coilcraft	DA2077–AL	No	

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